

TVL S143 02 AC0 Engineering Specification

1. Scope

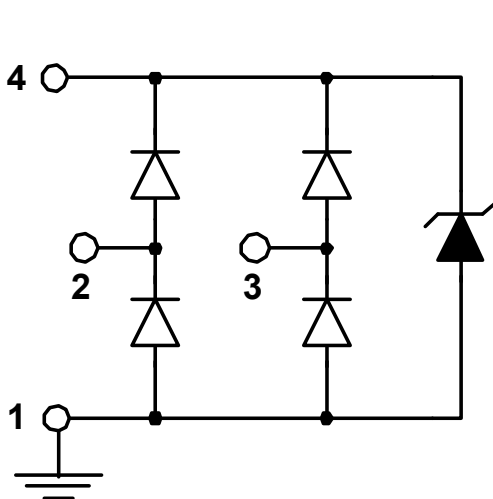
TVL S143 02 AC0's are TVS arrays designed to protect high-speed signal lines from overvoltage hazard of Electrostatic Discharge (**ESD**), Electrical Fast Transients (**EFT**) and **Lightning**. These interfaces can be used for USB2.0 power and data lines protection, notebook and personal computers, monitors and flat panel displays, IEEE 1394 Firewire ports, etc. The ESD protection of TVS arrays meets the immunity standard of IEC 61000-4-2, level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

2. Explanation of Part Number

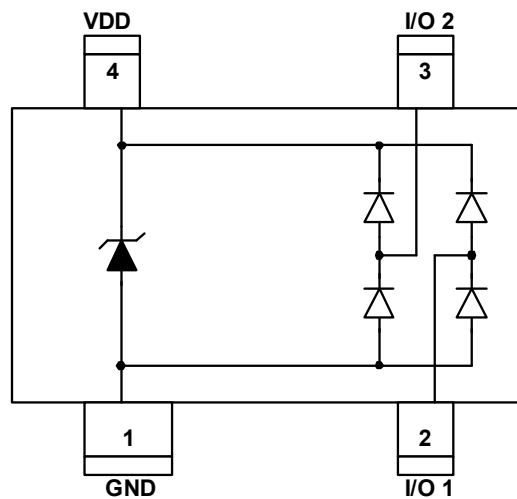
<u>TV</u>	<u>L</u>	<u>S143</u>	<u>02</u>	<u>AC0</u>
(1)	(2)	(3)	(4)	(5)

- (1) Product Type : TV=TVS Diode
- (2) Capacitance Code : L=Low Capacitance
- (3) Package Size Code
- (4) Channel Code : 02=2 Channels
- (5) Specialized Specification Code

3. Circuit Diagram /Pin Configuration



Circuit Diagram



Pin Configuration
SOT143-4L (Top View)

4. Specifications

4.1. ABSOLUTE MAXIMUM RATINGS

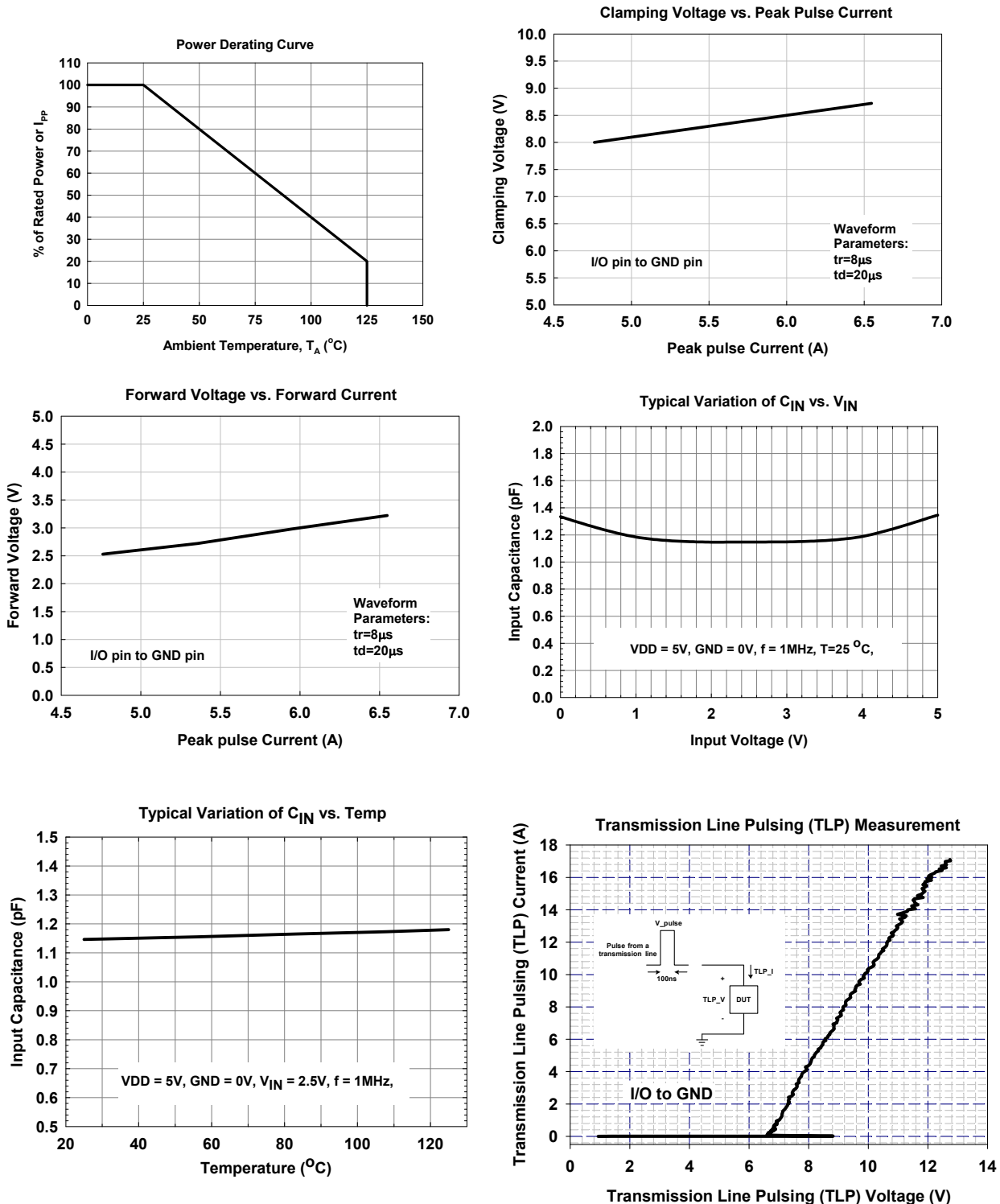
PARAMETER		PARAMETER	RATING	UNITS
Peak Pulse Power ($t_p = 8/20$ s)		P_{PP}	150	W
Peak Pulse Current ($t_p = 8/20$ s)		I_{PP}	5	A
ESD per	IEC 61000-4-2 (Air)	V_{ESD1}	+/-15	kV
	IEC 61000-4-2 (Contact)	V_{ESD2}	+/-12	kV
Operating Temperature		T_{opr}	-55 to +125	°C
Storage Temperature		T_{Stg}	-55 to +150	°C

Notes: Pins are plated with pure tin.

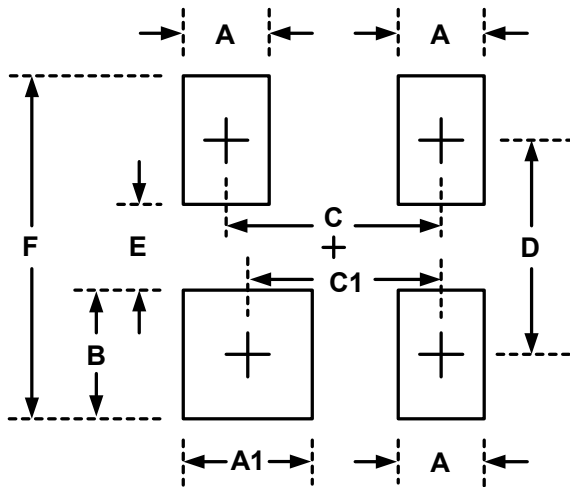
4.2. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to Ground			5	V
Reverse Leakage Current	I_R	$V_{RWM} = 5V$, $T = 25^\circ C$, Any I/O pin to Ground			1	μA
Reverse Breakdown Voltage	V_{BR}	$I_{BV} = 1mA$, Any I/O pin to Ground	6			V
ESD Clamping Voltage -I/O	V_{C1}	$I_{PP} = 1A$, $t_p = 8/20\mu S$, Any I/O pin to Ground		8.5	12.0	V
Reverse ESD Clamping Voltage -I/O	V_{C2}	$I_{PP} = 1A$, $t_p = 8/20\mu S$, Any I/O pin to Ground		1.8		V
Channel to Channel Input Capacitance	C_{J1}	$V_R = 0V$, $f = 1MHz$, Any I/O pin to Ground		0.6	0.7	pF
Channel I/O to GND Capacitance	C_{J2}	$V_R = 0V$, $f = 1MHz$, Any I/O pin to Ground		1.2	1.4	pF

4.3. TYPICAL CHARACTERISTICS



5. LAND LAYOUT



Dimensions		
Index	Millimeter	Inches
A	1.00	0.039
A1	1.40	0.055
B	1.40	0.055
C	1.92	0.076
C1	1.72	0.068
D	2.20	0.087
E	0.80	0.031
F	3.60	0.141

Notes: This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

6. Application information

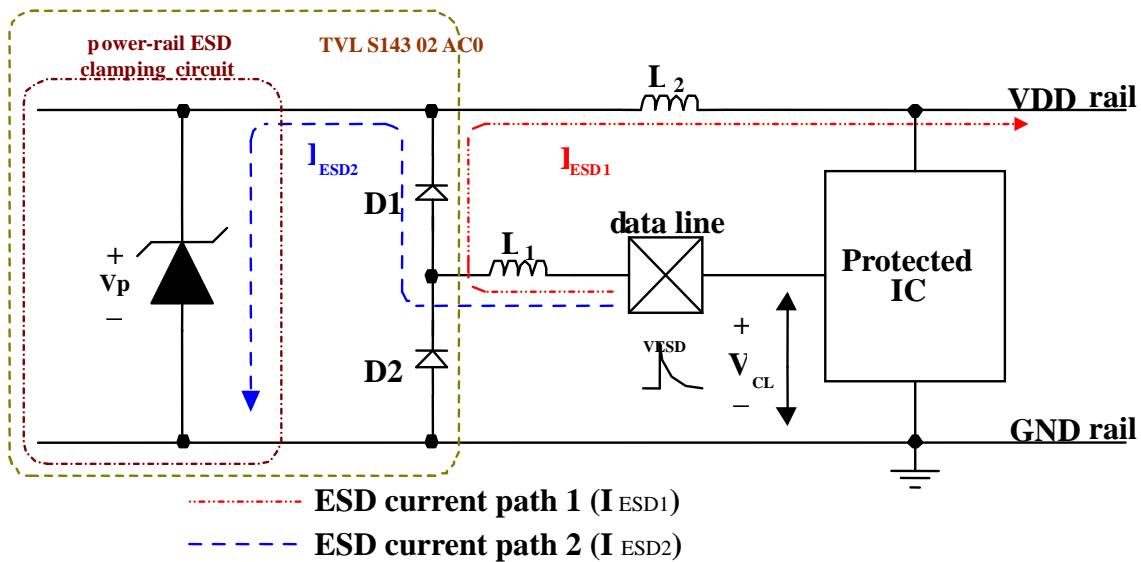
The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

$$V_{CL} = \text{Fwd voltage drop of D1} + \text{Breakdown voltage drop of D3} + \text{supply voltage of VDD rail} + L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

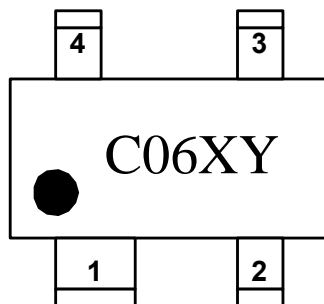
An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL} ! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The TVL S143 02 AC0 has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.



7. MARKING CODE

Marking Code: C06XY



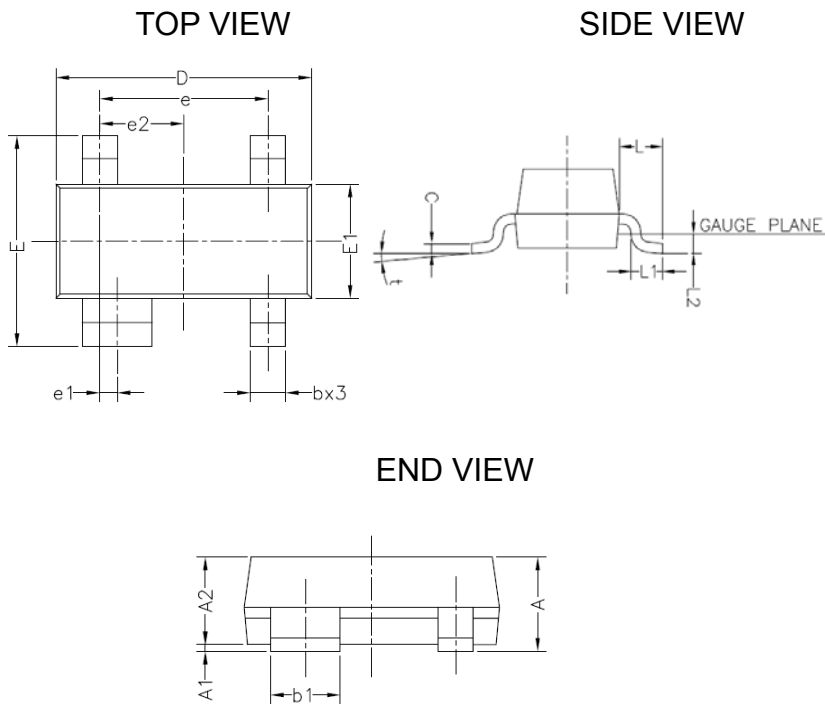
C06= Device Code

X= Date Code

Y=Control Code

8. Mechanical Details

SOT-143-4L PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.15	0.036	0.045
A1	0	0.1	0.000	0.004
A2	0.9	1.05	0.036	0.042
b	0.3	0.5	0.012	0.020
b1	0.75	0.90	0.030	0.036
C	0.08	0.15	0.003	0.006
D	2.8	3.00	0.111	0.119
E1	1.2	1.4	0.047	0.055
E	2.25	2.55	0.089	0.101
e1	0.20 BSC		0.0079 BSC	
e2	0.95 BSC		0.0375 BSC	
e	1.8	2.00	0.071	0.079
L	0.55 REF.		0.0217 BSC	
L1	0.3	0.5	0.012	0.020
L2	0.25 REF		0.0099 BSC	
t	0~8°		0~8°	

8.1. Taping Quantity: 3000pcs/ Tube